REMARKS

The Examiner is thanked for the thorough examination of the present application and the indication that claims 5, 7, 10, 11, 14, and 18-20 contain allowable subject matter. Claims 1-20 remain in this application. Claims 1 and 15 have been amended by adding the phrases "having a cell matrix" and "disposed outside the cell matrix." Support for the amendment is provided in the originally filed application at least in line 4 of paragraph 024, wherein LCD 12 includes a data driver 16, a scan driver 18 and a matrix of cells 20, and in FIGs. 1, wherein the transistors (element 26) and the second capacitors (element 24) are disposed outside the cell matrix.

For at least the reasons set forth herein, Applicant respectfully requests that the Examiner reconsider and withdraw the rejections.

Claim rejections

Claims 1-4, 6, 8, 9, 12, 13, and 15-17 were rejected under 35 U.S.C. 102(e) as allegedly anticipated by Maruoka et al. (U.S. Patent Publication No. 2002/0186192 A1), hereinafter Maruoka. For at least the following reasons, Applicant disagrees.

As amended, claim 1 recites:

> 1. A power-saving circuit for an active matrix liquid crystal display ("LCD") panel *having a cell matrix*, comprising:
>
> a plurality of first capacitors, each first capacitor corresponding to a data line of the LCD panel for collecting electrical charge provided on an associated data line;
>
> at least one set of second capacitors *disposed outside the cell matrix*;
>
> at least one set of transistors *disposed outside the cell matrix*, each transistor of a set corresponding to one of the plurality of first capacitors; and
>
> at least two control signals, each control signal corresponding to a set of the at least one set of transistors and corresponding to a set of the at least one set of second capacitors, and each control signal functioning to switch between a first and a second state to control the operation state of an associated set bf transistors,
>
> wherein the at least two control signals switch to a first state in a first sequence starting from a first control signal to a last control signal, and then in a

second sequence starting from the last control signal to the first control signal, the first sequence alternating with the second sequence.

(*Emphasis added.*) Claim 1 patently defines over the cited art for at least the reason that the cited art fails to disclose those features emphasized above.

As emphasized above, claim 1 defines a power-saving circuit for an active matrix liquid crystal display ("LCD") panel having a cell matrix, comprising: a plurality of first capacitors, each first capacitor corresponding to a data line of the LCD panel for collecting electrical charge provided on an associated data line; at least one set of second capacitors disposed outside the cell matrix; at least one set of transistors disposed outside the cell matrix, each transistor of a set corresponding to one of the plurality of first capacitors; and at least two control signals, each control signal corresponding to a set of the at least one set of transistors and corresponding to a set of the at least one set of second capacitors, and each control signal functioning to switch between a first and a second state to control the operation state of an associated set bf transistors, wherein the at least two control signals switch to a first state in a first sequence starting from a first control signal to a last control signal, and then in a second sequence starting from the last control signal to the first control signal, the first sequence alternating with the second sequence.

Maruoka fails to teach or suggest either "at least one set of second capacitors (analogized by Examiner to "second capacitor 54" shown in FIG. 34 of Maruoka) disposed outside the cell matrix" or "at least one set of transistors (analogized by Examiner to "active element 30" shown in FIG. 33 of Maruoka) disposed outside the cell matrix, such that each transistor of a set corresponding to one of the plurality of first capacitors," as the "second capacitor 54" and "active element 30" disclosed by Maruoka are not disposed outside the cell matrix as the application but disposed in the pixel portions (which is analogous to the cell matrix in the application).

For at least this reason, claim 1 is allowable over the cited reference. Insofar as claim 1 is allowable, dependent claims 2-4, 6, and 8 are also allowable on their own merits in claiming additional elements not included in claim 1.

Independent claim 9 recites:

> 9. A power-saving circuit for an active matrix liquid crystal display ("LCD") panel, comprising:
>
> a plurality of first capacitors, each first capacitor corresponding to a data line of the LCD panel for collecting electrical charge provided on an associated data line;
>
> a plurality of second capacitors;
>
> ***a plurality of transistors, each transistor including a gate, a first terminal coupled to one of the plurality of first capacitors, and a second terminal coupled to one of the plurality of second capacitors***; and
>
> a control signal coupled to the gates of the plurality of transistors, and functioning to switch between a first and a second state to control the operation state of the plurality of transistors,
>
> wherein each second capacitor in response to a first state of the control signal reaches a voltage level that is an average of a voltage level of the each second capacitor held at a previous first state of the control signal and a voltage level of an associated first capacitor in proportion to the capacitance values of the each second capacitor and the associated first capacitor.

(*Emphasis added.*) Claim 9 patently defines over the cited art for at least the reason that the cited art fails to disclose those features emphasized above.

Significantly, Maruoka fails to teach or suggest "a plurality of transistors (analogized by Examiner to "transistor 30" shown in FIG.33 of Maruoka), each transistor including a gate, a first terminal coupled to one of the plurality of first capacitors, and a second terminal coupled to one of the plurality of second capacitors," since "transistor 30" disclosed by Maruoka has only one terminal coupled to the capacitor, different from the transistors of the application having multiple terminals coupled to the capacitors.

For at least this reason, claim 9 is allowable over the cited reference. Insofar as claim 9 is allowable, claims 12 and 13 both depending from claim 9 are also allowable on their own merits in claiming additional elements not included in claim 9.

With regard to independent claim 15, as amended claim 15 recites:

> 15. A method of power saving for an active matrix liquid crystal display ("LCD") panel ***having a cell matrix***, comprising:
> providing a plurality of first capacitors;
> electrically coupling each first capacitor to a data line of the LCD panel;
> providing at least one set of transistors ***disposed outside the cell matrix***;
> electrically coupling each transistor of a set to one of the plurality of first capacitors;
> providing at least one set of second capacitors ***disposed outside the cell matrix***;
> electrically coupling each set of second capacitors to a set of transistors;
> providing at least one control signal;
> electrically coupling each control signal to a set of transistors, each control signal functioning to switch between a first and a second state to control the operation state of an associated set of transistors;
> switching the at least one control signal to a first state in a first sequence starting from a first control signal to a last control signal such that voltage levels of a second capacitor and an associated first capacitor are averaged in proportion to their respective capacitance values; and
> switching the at least one control signal in a second sequence starting from the last control signal to the first control signal such that voltage levels of a second capacitor and an associated first capacitor are averaged in proportion to their respective capacitance values.

(*Emphasis added.*) Claim 1 patently defines over the cited art for at least the reason that the cited art fails to disclose those features emphasized above.

Claim 15 defines a method of power saving for an active matrix liquid crystal display ("LCD") having defining features similar to those of claim 1. Specifically, claim 15 defines a panel having a cell matrix, comprising: providing a plurality of first capacitors; electrically coupling each first capacitor to a data line of the LCD panel; providing at least one set of transistors disposed outside the cell matrix; electrically coupling each transistor of a set to one of

the plurality of first capacitors; providing at least one set of second capacitors disposed outside the cell matrix; electrically coupling each set of second capacitors to a set of transistors; providing at least one control signal; electrically coupling each control signal to a set of transistors, each control signal functioning to switch between a first and a second state to control the operation state of an associated set of transistors; switching the at least one control signal to a first state in a first sequence starting from a first control signal to a last control signal such that voltage levels of a second capacitor and an associated first capacitor are averaged in proportion to their respective capacitance values; and switching the at least one control signal in a second sequence starting from the last control signal to the first control signal such that voltage levels of a second capacitor and an associated first capacitor are averaged in proportion to their respective capacitance values.

In contrast, Maruoka fails to teach or suggest either "providing at least one set of transistors (analogized by Examiner to "active element 30" shown in FIG.33 of Maruoka) disposed outside the cell matrix" or "providing at least one set of second capacitors (analogized by Examiner to "second capacitor 54" shown in FIG.34A of Maruoka) disposed outside the cell matrix, as the "second capacitor 54" and "active element 30" disclosed by Maruoka are not disposed outside the cell matrix (as the defined by the claimed embodiment) but rather are disposed in the pixel portions (analogous to the cell matrix of the present application).

For at least this reason, claim 15 is allowable over the cited reference. Insofar as claim 15 is allowable, dependent claims 16 and 17 are also allowable on their own merits in claiming additional elements not included in claim 15.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

By: _____

Daniel R. McClure
Registration No. 38,962

Thomas, Kayden, Horstemeyer & Risley, LLP
100 Galleria Pkwy, NW
Suite 1750
Atlanta, GA 30339
770-933-9500